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(54) Terminating dislocations in semiconductor epitaxial layers

(57) A semiconductor assembly comprising a substrate 11 and a lattice parameter mismatched epitaxial layer (5, 7) is arranged such that dislocations (3) which span the epitaxial layer, are terminated by dislocation termination regions (10) constructed in the epitaxial layer. A region of the semiconductor assembly is thus provided having a reduced number of dislocations. Dislocation termination regions may be provided by mesas or trenches in the substrate, or regions of the substrate rendered amorphous by high dosage ion implantation, for example.

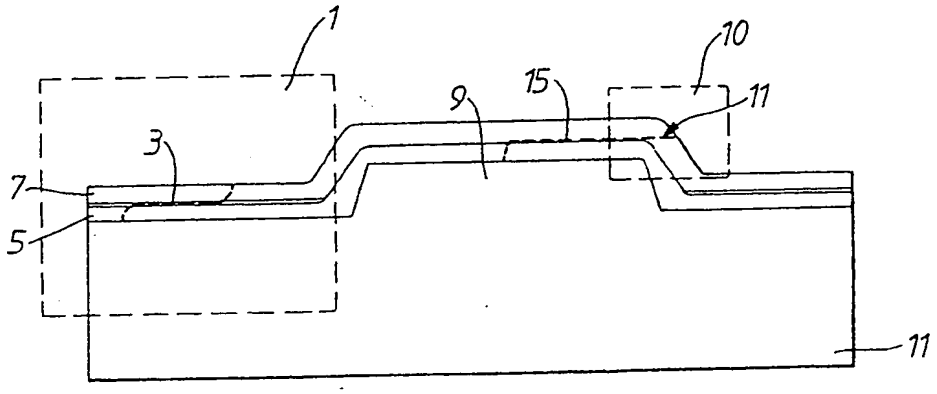

Fig.1.

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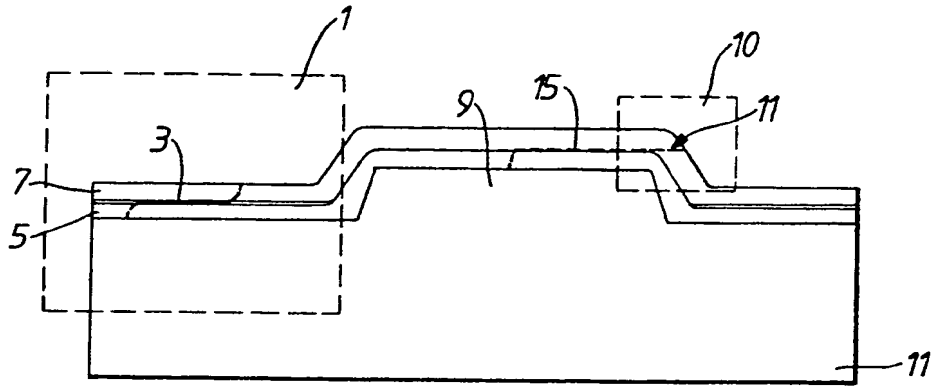

Fig.1.

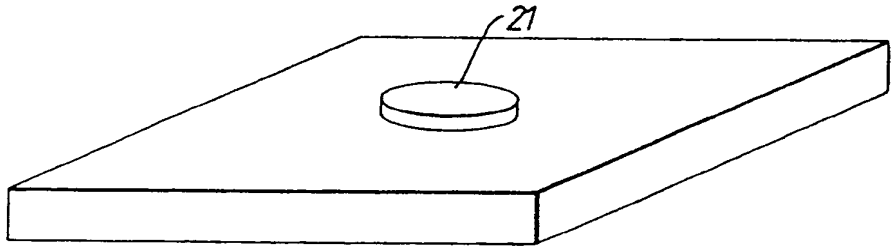

Fig.2.

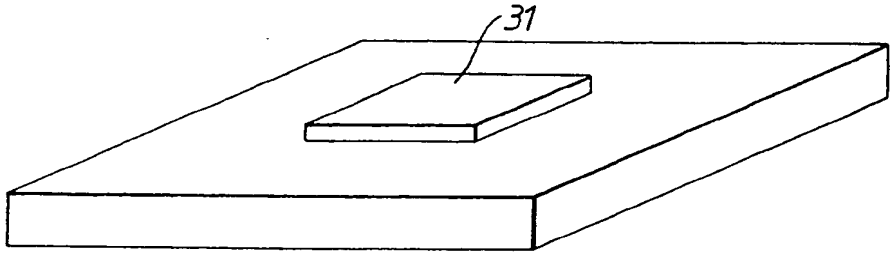

Fig.3.

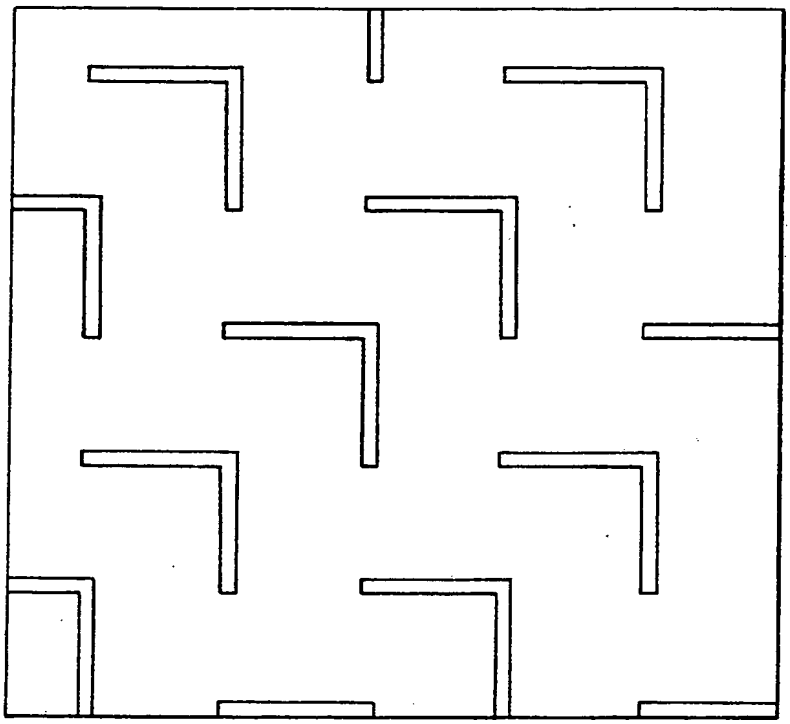

Fig.4.

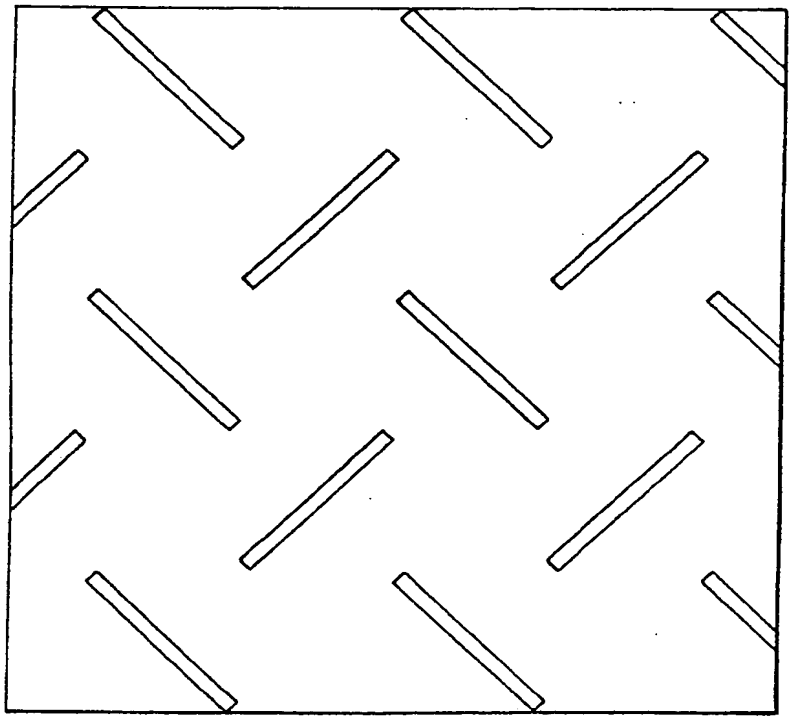

Fig.5.

A SEMICONDUCTOR ASSEMBLY

The present invention relates to a semiconductor assembly and more particularly to such an assembly comprising a substrate with at least one epitaxial layer thereupon.

When an epitaxial layer is grown upon a substrate and there is a lattice parameter mismatch then dislocations are produced near the interface between the layer and the substrate. This will in general be true for all types of semiconductor system, including Si, Ge, III-V materials, II-VI materials or IV-IV-VI materials for either epitaxial layers or substrates. Specific examples of such substrate/epitaxial layer mismatch are Ge on Si, GaAS on Si, InGaAs on GaAs, InP on GaAs, InP on Si, InGaAs on Si and GaAs on InP. These lattice-parameter-mismatch relieving dislocations although often produced in the vicinity of the lattice mismatch interface, have a strong tendency to interact to form perpendicular dislocations which span or thread across the grown or growing epitaxial layer. These perpendicular dislocations, in particular; lead to a severe degradation of the epitaxial layer's structural properties which in turn will effect electronic and optical properties. Degradation of the epitaxial layer results in impaired performance of electronic, optoelectronic or optical devices constructed using the epitaxial layer.

There is frequently a requirement to produce relatively thick epitaxial layers upon lattice-parameter-mismatched substrates. The relief of lattice parameter mismatches inevitably involves the formation of dislocations. It is however, the perpendicular

dislocations that span the epitaxial layer which present the greatest problem.

Previously, several approaches have been made to prevent or to hinder these perpendicular dislocations spanning the epitaxial layer. A first approach is to provide layers of graded lattice parameter material or strained layer super lattices in the epitaxial layer in order that the number of perpendicular dislocations spanning the epitaxial layer is reduced. Alternatively, layers of differing elastic properties in the epitaxial structure may be used. Furthermore, differing thermal treatments may be used to anneal out the dislocations.

These previous approaches reduce the number of dislocations entering higher regions of the epitaxial layer. However, this is at the expense of altering the configuration of the dislocation structures. Consider Figure 1, in part illustrating prior dislocation problems and in part illustrating the present invention. In a prior dislocation region 1, a spanning dislocation 3 is illustrated between epitaxial layers 5, 7, having respectively graded lattice parameters in accordance with the prior dislocation hindering approach described above. It may be considered that the dislocations have been "turned-out" into a direction substantially perpendicular to the epitaxial layer direction of deposition or growth. Thus, these dislocations might be expected not to adversley effect the epitaxial layer as they do not enter the higher regions of the epitaxial layer used to form electronic devices. In practise, however, subsequent influences upon the dislocation, possibly involving interactions between closely spaced adjacent dislocations, tend to redirect

dislocations into a mode where the dislocation is deflected to span the higher epitaxial layers. Consequently, in Figure 1, dislocation 3 is deflected at A such that it spans not only epitaxial layer 5, but also layer 7.

It is an objective of the present invention to provide a region of epitaxial layer upon a substrate of mismatched lattice parameter, wherein that region of epitaxial layer is substantially free of dislocations that span the epitaxial layer.

According to the present invention there is provided a semiconductor assembly comprising a substrate and, superjacent thereto at least one mismatched parameter layer whereby dislocations may be formed extending parallel to said layer, characterised in that the surface of the substrate is conformed to provide predetermined regions of facile dislocation termination whereat the parallely extending dislocations may terminate.

Further in accordence with the present invention there is provided in the manufacture of semiconductors, a method of reducing dislocations in mismatched parameter layers formed on a substrate, comprising a step of conforming the substrate to provide predetermined facile dislocation termination regions whereby dislocations in the structure, extending parallel to the layers thereof, tend to terminate in said regions.

An embodiment of the present invention will now be described by way of example only with reference to the accompanying drawings, where:-

Figure 1 illustrate, in cross-section, a semiconductor assembly according to the present invention;

Figure 2 illustrates, in perspective a first semiconductor substrate configuration in accordance with the present invention as illustrated in Figure 1;

Figure 3 illustrates, in perspective, a second semiconductor substate configuration in accordance with the present invention as illustrated in Figure 1;

Figure 4 illustrates, in plan, a third semiconductor substrate configuration in accordance with the present invention as illustrated in Figure 1; and,

Figure 5 illustrates, in plan, a fourth semiconductor substrate configuration in accordance with the present invention as illustrated in Figure 1.

In Figure 1 a semiconductor assembly according to the present invention is illustrated. As described previously in an epitaxial layer region 1 there is a likelyhood of dislocation 3 spanning the epitaxial layers 5, 7, as the dislocation 3 propagates until terminated at an outer or free surface of the epitaxial layer. It is an aspect of the present invention to provide facile dislocation or termination regions at predetermined locations such that a dislocation can be terminated in a relatively short distance of propagation. A raised section or mesa 9 in substrate 11 can be used to form a facile dislocation termination region 10. The mesa 9 can be formed by etching away surrounding substrate and may be, for example, circular or rectangular in plan. The size of the mesa 9 is determined by the function of the facile dislocation termination region 10; there should be sufficient curvature the of dislocation in the epitaxial layers 5, 7 to precipitate termination of the dislocation. A typical mesa 9 would

thus be 200μm across with a height of a 4μm. The height of the mesa 9 must be significant compared to the epitaxial layer 5, 7 thickness, although shape, width and height are not specifically critical.

The dislocation termination region 10 comprises the layers of epitaxial material about the mesa 9 edges, the underlying substrate mesa 9 acting to accentuate the grading of the layers of epitaxial material in the termination region 10. The nett result of accentuating the grading of the layers of epitaxial material 5, 7 is to make propagation of the dislocation 15 towards a free or amorphous outer surface 11 of the termintion region 10 most favourable. Propagation of the dislocation 15 is terminated at the surface 11.

A dislocation 15 in the region of epitaxial layer 5, 7 above the mesa 9 will be "turned over" as previously described. This "turned over" dislocation 15 will propagate in a less harmful lateral direction, most usually at the interface between adjacent graded epitaxial layers 5, 7, until it encounters an outer surface 11 of a facile dislocation termination region 10. At the termination region 10 the dislocation 15 tends to be attracted to the "free" external surface 11 of the region 10 thus terminating the dislocation 15 without becoming perpendicular to the substrate surface. It is thus important to arrange that the mesa 9 is dimensioned whereby the lateral distance travelled by the dislocation 15 is limited such that the possiblity of deflection of the dislocation into the perpendicular is reduced. It should be appreciated that it is not essential as dislocations may naturally propagate in a direction parallel to the substrate surface.

Although a mesa 9 is illustrated in Figure 1 it will be appreciated that a trench could be used instead to provide dislocation termination at its corners. Furthermore, dislocation sinks could be provided by alternative means other than etching structures into the substrate. An example of such an alternative means could be amorphous regions of semiconductor substrate as produced by high dosage ion implantation.

The present invention requires adaptation of the substrate or epitaxial layer in order to provide dislocation "sinks" or terminating regions 10. By such an approach or assembly the extent of dislocation propagation can be localised and the possibility of a dislocation spanning the epitaxial layer, perpendicularly to the useful surface thereof, is reduced.

Figures 2 to 5 illustrate examples alternative substrates mesa structure in accordance with the present invention. Figure 2 illustrates a raised circular mesa 21 whilst Figure 3 illustrates a similar raised square mesa 31, these mesa 21, 31 may be fabricated by etching away surrounding substrate material. In Figures 5 and 6 alternative patterning, by way of trenches, for the substrate is illustrated which allow greater use of the substrate for electronic device fabrication whilst ensuring a short distance between dislocation termination regions. It will be appreciated that mesa and trench structures in the present invention are interchangeable.

It will be appreciated that dislocation termination regions are preferably located such that these regions are maximised in the direction of most likely dislocation propagation.

In the present invention, whilst the number and effect of dislocations is reduced, the invention does not attempt to prevent dislocation nucleation.

CLAIMS:

1. A semiconductor assembly comprising a substrate and, superjacent thereto, at least one mismatched parameter layer whereby dislocations may be formed extending parallel to said layer, characterised in that the surface of the substrate is conformed to provide predetermined regions of facile dislocation termination whereat the parallely extending dislocations may terminate.

2. A semiconductor assembly as claimed in claims 1 wherein the mismatched parameter layer is arranged to turn non-parallel dislocations to extend parallel to the layer.

3. A semiconductor assembly as claimed in claim 2 wherein the mismatched parameter layer comprises a plurality of graded lattice parameter mismatched layers.

4. A semiconductor assembly as claimed in claim 2 wherein the mismatched parameter layer comprises a plurality of strained lattice parameter mismatched layers.

5. A semiconductor assembly as claimed in claim 2 wherein the mismatched parameter layer comprise a plurality of different elasticity constant layers.

6. A semiconductor assembly as claimed in claim 2 wherein the mismatched parameter layer comprises a single layer of traverse graded lattice parameter material.

7. A semiconductor assembly as claimed in claim 1, wherein the facile dislocation termination region is provided by a raised area upon the substrate.

8. A semiconductor assembly as claimed in claim 1, wherein the facile dislocation termination region is provided by a trench in the substrate.

9. A semiconductor assembly as claimed in claim 1, wherein the facile dislocation termination regions is provided by an amorphous semiconductor region in the substrate.

10. A semiconductor assembly as claimed in claim1 wherein the mismatched parameter layer comprises a plurality of discrete layers of material with graded respective lattice parameter values, such that any perpendicular dislocations are turned at the interface between said discrete layers.

11. A semiconductor assembly as claimed in claim 7 or 8 wherein the mesa or trench is formed by etching.

12. A semiconductor assembly as claimed in any proceding claim wherein the substrate and epitaxial layer are selected from the

following, Silicon, Germanium, III-V material, II-VI material or IV-IV-VI material.

13. A semiconductor assembly as claimed in any proceding claim wherein the substrate and epitaxial layer are respectively of the following, Germanium upon Silicon, Gallium Arsenide upon Silicon, Indium Gallium Arsenide upon Gallium Arsenide, Indium Phosphide upon Silicon, Indium Gallium Arsenide upon Silicon, or Gallium Arsenide upon Indium Phosphide.

14. A semiconductor assembly substantially as hereinbefore described with reference to the accompanying drawings.

15. In the manufacture of semiconductors, a method of reducing dislocations in mismatched parameter layers formed on a substrate, comprising the step of conforming the substrate to provide predetermined facile dislocation termination regions whereby dislocations in the structure, extending parallel to the layers thereof, tend to terminate in said regions.

16. A method of reducing dislocations spanning graded lattice parameter mismatched layers substantially as hereinbefore described.

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